A Virtual Memory Mini-Computer System

This is an abstract of a talk which will be presented at the 10th Annual Symposium On System Theory (South-Eastern Conference) sponsored by IEEE and North Carolina State and Duke Universities on March 22 and 23 of 1973.

The implementation (1) and simulation of a virtual memory multi-programmed operating system to support experiments in various laboratories and provide computing facilities to a community of users on a mini-computer with a modest amount of core will be described. The computer is a DDP-516 computer with 12K of 16-bit words (8K core and 4K MOS) and a cycle time of 0.96 usec. A 512K word fixed-head disk with 64 tracks and a 1800 RPM rotational speed provides the secondary storage capacity for the system. Computing power is distributed to the various labs by means of an I/O loop (2) connected to the computer via a send/receive interface. Devices are connected to the coaxial cable loop by means of a node terminal which consists of a repeater, node modem and a device interface. Maximum distance between repeaters is 500 feet. The bit rate on the loop is 3 megacycles. Up to 64 devices may be connected to the loop.

Of the 12K memory available, 4K is used for the bolted-in system code and 8K is used for user programs. The system code manages memory, handles all standard low-level interrupts and supports virtual addressing by converting virtual addresses to physical memory addresses. User programs consist of segments which are named blocks of storage. This gives the user an infinite address space available for his programs. Transfers between program segments are made by means of the CALL and GOTO macro-instructions which are assembled into two word virtual addresses consisting of an internal segment ID number and a relative address within the program segment being transferred to. Higher level storage is provided for the user by means of named files which consist of linked fixed length segments. Segment boundaries are invisible to the user. Virtual memory addressing modes, memory management and disk management strategies will be discussed in some detail in the body of this talk.

During the early phase of the design of the operating system, a complete simulation of the system was carried out to better understand the inner workings of the system and to determine the bottlenecks which limit throughput and response. Programmable megacycle clocks were installed on the computer to permit routines to be timed accurately. This enabled one to divide real time into three components, system, user and idle time. These times are integrated and displayed on meters to give dynamic readings. Simulation results agreed very closely with

measurements made directly on the system by means of the programmable clocks. The simulation model was then extended to study the effects of increasing memory size, disk speed and memory speed for this system. The results were incorporated into an economic model of the system pointing out the cost effectiveness of the improvements. Memory management strategy and user file organization were found to be the two major factors affecting the throughput and response of the operating system.

Some of the current uses of the system will be discussed. The system is capable of handling up to 12 simultaneous users in the 8K of memory available to the users. The low memory profile of each user is made possible by the segmentation of a user's program. A language similar to FORTRAN and BASIC has been designed specifically for a virtual memory environment to provide calculation capabilities to the community of users. The virtual memory concept allows one to write a much larger program than would normally fit into 8K of memory. The system also serves as a remote job entry point for submitting batch jobs to the central computing facility, such as listings, punching card decks, FORTRAN jobs, etc. A variety of mini-computers are connected to the I/O loop for various experiments in the lab. In particular one node on the I/O loop is connected to a message switching machine. This enables one to communicate with any other computer which may be connected to the network controlled by the switching machine. Currently a large file system is maintained on a PDP 11/45 computer on the network. This provides readily available secondary storage and back-up facilities for the rather limited file storage capabilities of the DDP-516 machine. Interactive graphics research is another facility supported by the DDP-516 I/O loop.

1. C. Christensen and A. D. Hause, "A Multiprogramming, Virtual Memory System for a Small Computer", AFIPS - Conference Proceedings, Vol. 36, 1970 Spring Joint Computer Conference.

2. D. R. Weller, "A Loop Communication System for I/O to a Small Multi-User Computer", 5th Annual 1971 IEEE International Computer Society Conference, September 1971.